IN THE CLAIMS:

Please cancel claims 1-8 without prejudice or disclaimer, and add new claims 13-18 as follows:

1-8. (Cancelled)

9. (Withdrawn) A method of testing a memory circuit which has a plurality of signal nodes to which an operation control signal for controlling memory selecting operation and an operation timing signal are supplied, and in which word-line selecting operation, sense amplifier operation following the word-line selecting operation, memory selecting operation including data transmitting operation, and the termination of the memory selecting operation including the termination of the word-line selecting operation are effected on the basis of the operation control signal, a reference timing of the internal operation of said memory circuit being set by the operation timing signal, comprising the steps of:

lowering a frequency of the timing signal at the time of test operation by a testing apparatus to a level lower than at the time of normal memory operation in correspondence with the performance of said testing apparatus; and

changing a period of operation by the operation control signal by combining the timing signal at the time of the test operation with a timing signal used exclusively for testing so as to test response characteristics of said memory circuit.

10. (Withdrawn) A method of testing according to claim 9, wherein said memory circuit has read/write memory cells, and effects the memory selecting operation including the word-line selecting operation based on the operation control signal and the operation of writing data into said memory cell selected by the word-line selecting operation, and wherein the period of operation of said memory circuit is changed by changing an input timing of the timing signal used exclusively for testing with respect to the timing signal, and the data write response characteristics of sad memory circuit are tested on the basis of the change of the

period of operation.

11. (Withdrawn) A method of testing according to claim 9, wherein upon termination of the memory selecting operation said memory circuit effects sequential operation including the termination of the word-line selecting operation and the reset operation for resetting to a predetermined level the potential of a bit line to which data for a memory cell is imparted, and a period up to a change timing of the operation control signal for starting next memory selecting operation is changed by changing an input timing of the timing signal used exclusively for testing, so as to test the response characteristics of the reset operation.

12. (Withdrawn) A method of manufacturing a memory circuit which has a plurality of signal nodes to which an operation control signal for controlling memory selecting operation and an operation timing signal are supplied, and in which word-line selecting operation, sense amplifier operation following the word-line selecting operation, memory selecting operation including data transmitting operation, and the termination of the memory selecting operation including the termination of the word-line selecting operation are effected on the basis of the operation control signal, a reference timing of the internal operation of said memory circuit being set by the operation timing signal, said memory circuit having a defect remedy circuit, comprising:

a first step of preparing a semiconductor integrated circuit substrate on which said memory circuit and said defect remedy circuit are formed;

a second step of testing response characteristics of said memory circuit by a testing apparatus by setting a frequency of the timing signal to a level lower than that at the time of normal operation in correspondence with the performance of said testing apparatus, by controlling a period of operation of said memory circuit through a combination of the timing signal and a timing signal used exclusively for testing, and by controlling the period of operation;

a third step of determining a portion of said memory circuit whose defect is to be

remedied on the basis of a result of the testing of the response characteristics; and

a fourth step of remedying by said defect remedy circuit the portion whose defect is to be remedied and which has been determined in the third step.

13. (New) A semiconductor integrated circuit device comprising:

a first terminal which receives a first clock signal outside of said semiconductor integrated circuit device;

a second terminal which receives an address signal outside of said semiconductor integrated circuit device;

a third terminal which receives a second clock signal outside of said semiconductor integrated circuit device, said second clock signal has a frequency lower than a frequency of said first clock signal;

a delay circuit which delays said address signal;

a control circuit which receives said first clock signal, said second clock signal, and said address signal, and outputs a control signal in accordance with whether said semiconductor integrated circuit is in a normal operation mode or a test mode for testing at least one of a write time and a bit-line percharge time; and

a memory circuit which receives said control signal, and includes a plurality of word lines, a plurality of bit lines, and a plurality of memory cells,

wherein in the normal operation mode, a selecting operation of one of said plurality of word lines is terminated by an output of said delay circuit,

wherein in the test mode, another selecting operation of one of said plurality of word lines operation is terminated by said second clock signal.

14. (New) A semiconductor integrated circuit device according to claim 13, wherein said control circuit controls a time during said one of a plurality of word lines is selected in the test mode to be longer than a time during said one of a plurality of word lines is selected in the normal operation mode.

15. (New) A semiconductor integrated circuit device according to claim 13,
wherein said control circuit includes a latch circuit and a flip-flop circuit,
wherein said flip-flop circuit receives said first clock signal and said address signal, and outputs said address signal to said delay circuit, and
wherein said latch circuit outputs said control signal and receives signals outputted from said flip-flop circuit and said delay circuit.

16. (New) A semiconductor integrated circuit device according to claim 14, wherein said memory circuit further includes a row decoder, a column decoder, and a sense amplifier.

17. (New) A semiconductor integrated circuit device according to claim 14, wherein said plurality of memory cells are DRAM memory cells.

18. (New) A semiconductor integrated circuit device according to claim 15, further comprising a circuit stored with information of whether said semiconductor integrated circuit device is in the normal operation mode or in the test mode.